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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/510,286	10/06/2004	Takakazu Yano	Q83707	7527

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EXAMINER	
PHAM, TAMMY T	
ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/510,286	YANO ET AL.	
	Examiner	Art Unit	
	TAMMY PHAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 2-3 have been cancelled. Claims 1, 4-12 are pending.

Response to Arguments

2. Applicant's arguments filed 17 January 2008 have been fully considered but they are not persuasive.

3. **In regards to amended independent claims 1 and 6,** Applicant submits that *"Neither Yano et al. or Takeshi discloses that the range of the potential of a pictogram is within the range of the potential of the common electrode (Remarks 8)."* Examiner respectfully disagrees. The range of the potential of a pictogram is clearly depicted (Fig. 2, terminals 159-160; column 4, lines 30-35) as having the same potential of the common electrode (Fig. 2, terminals 1-158; column 4, lines 20-25). Although Yano may not explicitly teach that the range of the potential of a pictogram is within the range of the potential of the common electrode, this can easily be inferred by one skilled in the art, that the potentials of both are the same (Fig. 2). Hence, one can conclude that the potential of the pictogram must be within the range of the common electrode.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano et al. (US Patent No: 6,515,645 B1) in view of Takeshi (Japanese Publication Number: 2000-003144).

5. **As for independent claim 1,** Yano teaches of a liquid crystal display device (Fig. 1) capable of displaying a moving image display area (Fig. 1, item 107) for displaying moving images and a pictogram display area (Fig. 1, item 108), wherein the moving image display area (Fig. 1, item 107) is formed by arranging display electrodes (Fig. 1, items 112-113) in a matrix, the display electrode (Id.), and the pictogram display area (Fig. 1, item 108) is formed by disposing a segment electrode (Fig. 1, items 110-111) in a shape of a predetermined pictogram, wherein

6. a common electrode (Fig. 1, items 122, 125) is provided on an entire position that is opposed to both the moving image display area (Fig. 1, item 107) and the pictogram display area (Fig. 1, item 108),

7. a scan-side integrated circuit (Fig. 1, item 103) for driving scan lines (Fig. 1, lines coming from item 103) is provided so as to be connected to the scan lines (Id.) arranged in a row direction in the moving image display area (Fig. 1, item 107),

8. a data-side integrated circuit (Fig. 1, item 104) for driving data lines (Fig. 1, lines coming from item 104) is provided so as to be connected to the data lines (Id.) arranged in a column direction in the moving image display area (Fig. 1, item 107), and the data-side integrated circuit (Fig. 1, item 104) is provided with a larger number of output terminals (Fig. 1, item 124) than the data lines (Fig. 1, lines coming out of item 104 and into area 107), and

9. the segment electrode (Fig. 1, items 110-111) is connected to an output terminal (Fig. 1, item 124), which is different from an output terminal (Id.) to which data line (Fig. 1, lines

coming out of item 104) for moving images is connected, of the data-side integrated circuit (Fig. 1, item 104), and a difference between a potential of the common electrode (Fig. 1, items 122, 125) and a potential of an output signal from the data-side integrated circuit (Fig. 1, item 104), which is generated due to driving based on polarity of the common electrode (Fig. 1, item 122, 125), is used to display the pictogram in the pictogram display (Fig. 1, item 108, column 4, lines 43-46) *(NOTE: Due to the broad claim language, Examiner will assume that "a potential" of the common electrode is zero and because the same data that is used for driving the animation area is also used to drive the pictogram area, it follows that a difference between the common electrode (having zero value) and the output signal of the data driver is used to drive the pictogram area),*

10. wherein an output signal from the data-side integrated circuit (Fig. 1, item 104) to the segment electrode (Fig. 1, items 110-111) is generated so that an output potential is varied for each predetermined period (Fig. 3; where each period is where the polarity inverses), and

11. wherein the output potential varied for each predetermined period (Fig. 1; where each period is where the polarity inverses) is made within a voltage range of the potential of the common electrode (Fig. 1, items 122, 125; Fig. 2, voltages for row 205 of electrodes 1-158), thereby inherently suppressing a direct-current component caused by a difference between the potential of the data output signal (Fig. 2, voltages for row 205 of electrodes 159-160) and the potential of the common electrode (Fig. 2, voltages for row 205 of electrodes 1-158) (this process inherently suppresses the current caused by a difference between the data and the common voltage because there is no difference between the data (Fig. 2, voltage to lines 159-160) and the common voltage (Fig. 2, voltage to lines 1-158)).

12. Yano fails to teach that the display electrodes are driven by TFTs or that the data and scan lines are connected to TFTs.

13. Takeshi teaches that the display electrodes (Drawing 4, electrodes part of item 4) are driven by TFTs (Drawing 4, item 9) or that the data (Drawing 4, item 11)and scan lines (Drawing 4, item 10) are connected to TFTs (Drawing 4, items 9, 12).

14. It would have been obvious to one with ordinary skill in the art at the time the invention was made to connect the TFTs of Takeshi with the display electrodes, data and scan lines of Yano; because TFTs are well recognized in the art for their capacity to allow each display electrode to be individually controlled, and hence control the amount of voltage coming in and as well as the voltage leaking out.

15. **As for independent claim 6,** in addition to the claim limitations of claim 1 above, Yano fails to further teach that the pictogram electrode (Fig. 1, items 110-111) ***being driven by a pictogram thin-film transistor element;*** wherein either one of a source terminal or a drain terminal of the pictogram thin-film transistor is connected to, among a plurality of output terminals (Fig. 1, item 124) of the data-side integrated circuit (Fig. 1, item 104).

16. Takeshi teaches that the pictogram electrode (Drawing 4, electrodes part of item 5) being driven by a pictogram thin-film transistor element (Drawing 4, item 12); wherein either one of a source terminal or a drain terminal of the pictogram thin-film transistor (Id.) is connected to, among a plurality of output terminals of the data-side integrated circuit (Drawing 4, item 14).

17. It would have been obvious to one with ordinary skill in the art at the time the invention was made to have either the source or drain terminal of the pictogram TFT connected to the data side integrated circuit; because TFTs are well recognized in the art for their capacity to allow each display electrode to be individually controlled, and hence control the amount of voltage coming in and as well as the voltage leaking out.

18. **As for claim 2,** Yano teaches of an output signal from the data-side integrated circuit (Fig. 1, item 104) to the segment electrode (Fig. 1, items 110-111) is generated so that an output potential is varied for each predetermined period (Fig. 3; where each period is where the polarity inverses).

19. **As for claim 3,** Yano teaches that the output potential varied for each predetermined period (Fig. 1; where each period is where the polarity inverses) is made within a voltage range of the potential of the common electrode (Fig. 1, items 122, 125), thereby suppressing a direct-current component caused by a difference between the potential of the data output signal and the potential of the common electrode.

20. **As for claim 4,** Yano teaches that the predetermined period (Fig. 3; where each period is where the polarity inverses) is a period required for inverting a polarity of the common electrode (Fig. 1, items 122, 125) (see column 4, lines 43-46).

21. **As for claim 5,** Yano teaches that the output potential varied for each predetermined period (Fig. 3; where each period is where the polarity inverses) is controlled by an input signal (Fig. 2) defining a gray tone to the data-side integrated circuit (Fig. 1, item 104, column 3, lines 65-1).

22. **As for claim 7,** Yano as modified by Takeshi above in claim 6, teaches that the pictogram display area (Takeshi, Drawing 4, item 5) is provided with a plurality of the pictogram electrodes (Takeshi, Drawing 4, electrodes associated with item 5) and a plurality of the pictogram thin-film transistors (Takeshi, Drawing 4, item 12), and gate terminals of the pictogram thin-film transistors (Id.) are connected to a same output terminal of the scan-side integrated circuit (Takeshi, Drawing 4, item 6). *(NOTE: The TFT (Takeshi, Drawing 4, item 12) of one row of the pictogram display area (Takeshi, Drawing 4, item 5) are all connected to the same output terminal of the scan-side integrated circuit (Takeshi, Drawing 4, item 6)).*

23. **As for claim 8,** Yano as modified by Takeshi above in claim 6, teaches that the gate terminals of the plurality of pictogram thin-film transistors (Takeshi, Drawing 4, item 12) are connected to different output terminals of the scan-side integrated circuit (Takeshi, Drawing 4, item 6). (NOTE: The TFT (Takeshi, Drawing 4, item 12) of each separate row of the pictogram display area (Takeshi, Drawing 4, item 5) are all connected to the same output terminal of the scan-side integrated circuit (Takeshi, Drawing 4, item 6)).

24. **As for claim 9,** Yano as modified by Takeshi above in claim 6, teaches that one pictogram electrode (Takeshi, Drawing 4, electrodes associated with item 5) has connected thereto a plurality of the pictogram thin-film transistors (Takeshi, Drawing 4, item 12*). (NOTE: How there are a plurality of TFT (Takeshi, Drawing 4, item 12) and the electrodes (Takeshi, Drawing 4, electrodes associated with item 5) are all interconnected with the TFT).*

25. **As for claim 10,** Yano as modified by Takeshi above in claim 9, teaches that the gate terminals of the plurality of pictogram thin-film transistors (Takeshi, Drawing 4, item 12) connected to the same pictogram electrode (Takeshi, Drawing 4, electrodes associated with item 5, where the electrodes is shared amongst the TFT is each column) is connected to different output terminals of the scan-side integrated circuit (Takeshi, Drawing 4, item 6).

26. **As for claim 11,** Yano as modified by Takeshi above in claim 6, teaches that of a gate terminal of the pictogram thin-film transistor (Takeshi, Drawing 4, item 12) is connected to, among a plurality of output terminals of the scan-side integrated circuit (Takeshi, Drawing 4, item 6), an output terminal that is different from output terminals to which scan lines (Takeshi, Drawing 4, item 10) connected to the moving image thin-film transistor (Takeshi, Drawing 4, item 9) are connected.

27. **As for claim 12,** Yano as modified by Takeshi above in claim 6, teaches that the pictogram display area (Takeshi, Drawing 4, item 5) is provided with the plurality of the pictogram electrodes (Takeshi, Drawing 4, electrodes associated with item 5) and the plurality of

the pictogram thin-film transistors (Takeshi, Drawing 4, item 12), and any one of source terminals and drain terminals, which are connected to the pictogram electrodes (Takeshi, Drawing 4, electrodes associated with item 5), of the plurality of the pictogram thin-film transistors (Takeshi, Drawing 4, item 12), are connected to a same output terminal of the data-side integrated circuit (Takeshi, Drawing 4, item 8), and other terminals of the plurality of pictogram thin-film transistors (Takeshi, Drawing 4, item 12), are connected to different output terminals of the scan-side integrated circuit (Takeshi, Drawing 4, item 6).

Conclusion

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

29. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TP
26 March 2008

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